PATENT APPLICATION

Xerox Docket No. D/A1591D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Jingkuang CHEN et al.

Application No.: 10/727,692 Examiner: L. SCHILLINGER

Filed: December 4, 2003 Docket No.: 111517.01

For: SYSTEMS AND METHODS FOR INTEGRATION OF HETEROGENEOUS CIRCUIT DEVICES

BRIEF ON APPEAL

Appeal from Group Art Unit 2813

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APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is our Brief on Appeal in the above-identified application.

The Commissioner is hereby authorized to charge Deposit Account No. 24-0037 in the amount of Five Hundred Dollars ($500.00) in payment of the Brief fee under 37 C.F.R. 41.20((b)(2). In the event of any underpayment or overpayment, please debit or credit our Deposit Account No. 24-0037 as needed in order to effect proper filing of this Brief.

Respectfully submitted,

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JAO:TJB/mab
Date: July 30, 2007

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DEPOSIT ACCOUNT USE AUTHORIZATION
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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application is Xerox Corporation, by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 012416, Frame 0410.

II. RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or that will directly affect or be directly affected by or have a bearing upon, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 4-13, 17-20 are on appeal.

Claims 1, 3-13 and 17-24 are pending.

Claims 1, 4-13 and 17-20 are rejected.

Claims 3 and 21-24 are withdrawn from consideration.

Claims 2 and 14-16 are canceled.

IV. STATUS OF AMENDMENTS

An Amendment After Final Rejection was filed on March 28, 2007. By an Advisory Action dated May 18, 2007, it was indicated that the requested amendments were not entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The below summary of the subject matter refers to the specification and drawings. Any reference to the specification and drawings below is only exemplary and should neither be construed to encompass every portion of the specification and drawings that supports the various claimed features nor construed to limit the claimed subject matter beyond the claim language.

The present application relates to circuit devices with a plurality of heterogeneous devices in a single substrate and methods for fabricating a plurality of such devices (paragraph [0001]; P1/L5-7). Figures 1-32 illustrate various steps of an exemplary embodiment of a method for fabricating a plurality of heterogeneous devices in a single substrate (paragraph [0030]; P6/L1-2).

Claim 13 is directed towards a heterogeneous device including a substrate 120 with a plurality of heterogeneous circuit devices defined in the same substrate by an implantation (Fig. 32 and paragraph [0031]; P6/L10-20). The plurality of heterogeneous circuit devices include at least one complementary metal oxide semiconductor (CMOS) transistor 140, at least one double-diffused metal oxide semiconductor (DMOS) transistor 150, and a photodiode 160 (Fig. 32 and paragraph [0031]; P6/L10-20).

The structure of the recited subject matter of claim 13 provides more efficient fabrication of devices including: reducing the cost for fabrication, reducing the size of the devices formed, and providing more accurate fabrication of the devices (paragraphs [0005]-[0008]; P2/L6-17). Thus, better signal-to-noise ratio and higher reliability and accuracy can be achieved (paragraph [0009]; P2/L18-19).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

1) Claim 13 is rejected as failing to comply with the written description requirement under 35 U.S.C. §112, first paragraph; and

2) Claims 1, 4-13 and 17-20 are rejected as anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,477,065 to Nakagawa.

VII. ARGUMENT

The Examiner rejects claim 13 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Additionally, the Examiner separately rejects claims 1, 4-13 and 17-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,477,065 to Nakagawa.

In these rejections, the Examiner has consistently and improperly applied the law relating to the written description requirement and anticipation. Proper application of the law demonstrates that claim 13 does comply with the written description requirement and that no *prima facie* case of anticipation has been established.

A. Claim 13 is Properly Supported in the Specification and Figures

The February 26, 2007 Final Rejection (hereinafter "Office Action") improperly rejects claim 13 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner improperly construes the claim language of claim 13 in view of the specification.

The Office Action asserts that the language in claim 13 "a plurality of homogenous devices defined in the same substrate by an implantation that include a CMOS and DMOS and a photodiode defined in the same substrate by the same implantation process" contradicts the specification because the specification discusses different ion implantations for the creation of the CMOS, DMOS and photodiode devices. Additionally, the Examiner misconstrues the language of claim 13 by asserting the language of claim 13 suggests a single implantation process which is a simultaneous process.

However, the specification in paragraph [0031] and Figure 32 discloses a CMOS transistor 140, a DMOS transistor 150 and a photodiode 160 combined in a single-crystal-silicon layer 110. When reading the specification as a whole, starting with Figure 1 and ending with Figure 32, the specification discloses the same implantation process that starts

with Figure 1 and results in Figure 32. Thus, the specification clearly provides support for the feature of "a plurality of homogenous devices defined in the same substrate by an implantation process, the plurality of heterogeneous circuit devices including at least one complimentary metal oxide semi-conductor (CMOS) transistor and at least one double-diffuse metal oxide semi-conductor (DMOS) transistor; and a photodiode defined in the same substrate by the same implantation process," as recited in claim 13.

B. Claims 1, 4-13 and 17-20 Are Not Anticipated By Nakagawa

1. The Office Action Misapplies the Anticipation Standard

The Office Action misapplies the anticipation standard in rejecting claims 1, 4-13 and 17-20 under 35 U.S.C. §102(b) by improperly combining and modifying different embodiments of the applied reference, U.S. Patent No. 5,477,065 to Nakagawa, to anticipate the features recited in claim 13.

To anticipate an invention, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim (See *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375 (Fed. Cir. 2001), *cert. denied*, 122 S.Ct. 1436 (2002). However, the reference "must clearly and unequivocally disclose the claimed compound or direct those skilled in the art to the compound without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkely*, 455 F.2d 586, 587, 172 USPQ 524 (CCPA 1972). Therefore, the Office Action cannot pick and choose elements from the tenth and eleventh embodiment of Nakagawa to anticipate the features recited in claim 13.

Nakagawa does not disclose all of the features of claim 13, the CMOS, DMOS and photodiode in a single embodiment in the same substrate, but instead discloses them in two separate embodiments. The Office Action improperly combines the tenth embodiment of Nakagawa, Fig. 12D, forming a CMOS and DMOS circuit with the eleventh embodiment,

Fig. 13A, a photodiode to conclude the reference teaches a CMOS and a DMOS circuit in combination with the photodiode on the same substrate by the same implantation process. However, the features of claim 13 are not "found in a single piece of prior art in exactly the same situation and united the same way to perform the identical function," *Sandisk Corp. v. Lexar Media, Inc.*, 91 F. Supp.2d 1327, 1336 (N.D. Calif. 2000), but are instead found in two separate embodiments. Thus, the Office Action picking and choosing different embodiments of Nakagawa to anticipate the features of claim 13 is clearly improper.

The Office Action asserts that the language of Nakagawa, in col. 8, lines 50-65, stating that the semiconductor element chip has one or more elements formed thereon in the same manner as in the other embodiments, supports the idea that the CMOS and DMOS taught in the other embodiments may be combined to be formed on the same substrate with the photodiode. Clearly, the standard for anticipation is not met with the broadly construed language that a semiconductor element chip can have one or more elements formed thereon. This broad statement does not meet the anticipation standard since it does not specifically teach a "plurality of heterogeneous circuit devices including at least one complimentary metal oxide semi-conductor (CMOS) transistor and at least one double-diffuse metal oxide semi-conductor (DMOS) transistor; and a photodiode defined in the same substrate by the same implantation process," as recited in claim 13. Since Nakagawa fails to teach elements that can reasonably be considered to correspond to the positively recited claim features arranged as in the claim, *i.e.* arranged on the same substrate, it does not anticipate the features recited in claim 13.

Therefore, the Office Action improperly rejects claim 13 under 35 U.S.C. §102(b) for being anticipated by Nakagawa because the Office Action misapplied the anticipation standard by improperly combining and modifying embodiments of Nakagawa to anticipate the features recited in claim 13.

VIII. CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1, 4-13 and 17-20 are in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the rejections of claims 1, 4-13 and 17-20.

Respectfully submitted,

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APPENDIX A - CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

1. The device of claim 13, further comprising:

a high voltage well of a first circuit device defined in the substrate; and

a first low voltage well of a second circuit device defined in the substrate.

4. The device of claim 1, wherein the substrate comprises a layer of silicon.

5. The device of claim 4, wherein the layer of silicon comprises p-type silicon.

6. The device of claim 1, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

7. The device of claim 6, wherein the single-crystal-silicon layer comprises p-type silicon.

8. The device of claim 1, further comprising a second low voltage well of the second circuit device defined in the substrate.

9. The device of claim 8, further comprising a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

10. The device of claim 9, further comprising a polysilicon gate associated with each of the high voltage well, the first low voltage well and the second low voltage well.

11. The device of claim 10, further comprising:

a P-body defined in the high voltage well of the first circuit device;

an N+ source/drain defined in each of the P-body, the high voltage well and the first low voltage well of the second circuit device; and

a P+ source/drain in each of the P-body and the second low voltage well of the second circuit device.

12. The device of claim 11, further comprising:

a passivation oxide layer over at least the field oxide layer and the polysilicon gates;

a plurality of vias through the passivation oxide layer; and

a plurality of contacts, each of the contacts extending through the vias and contacting at least one of the sources/drains.

13. A heterogeneous device, comprising:

a substrate;

a plurality of heterogeneous circuit devices defined in the same substrate by an implantation, the plurality of heterogeneous circuit devices including at least one complementary metal oxide semiconductor transistor and at least one double-diffused metal oxide semiconductor transistor; and

a photodiode defined in the same substrate by the same implantation.

17. The device of claim 13, wherein the substrate comprises a layer of silicon.

18. The device of claim 17, wherein the layer of silicon comprises p-type silicon.

19. The device of claim 13, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

20. The device of claim 19, wherein the single-crystal-silicon layer comprises p-type silicon.

APPENDIX B - EVIDENCE APPENDIX

A copy of each of the following items of evidence relied on by the Appellant and/or the Examiner is attached:

NONE

APPENDIX C - RELATED PROCEEDINGS APPENDIX

Copies of relevant decisions in the following related proceedings are attached:

NONE